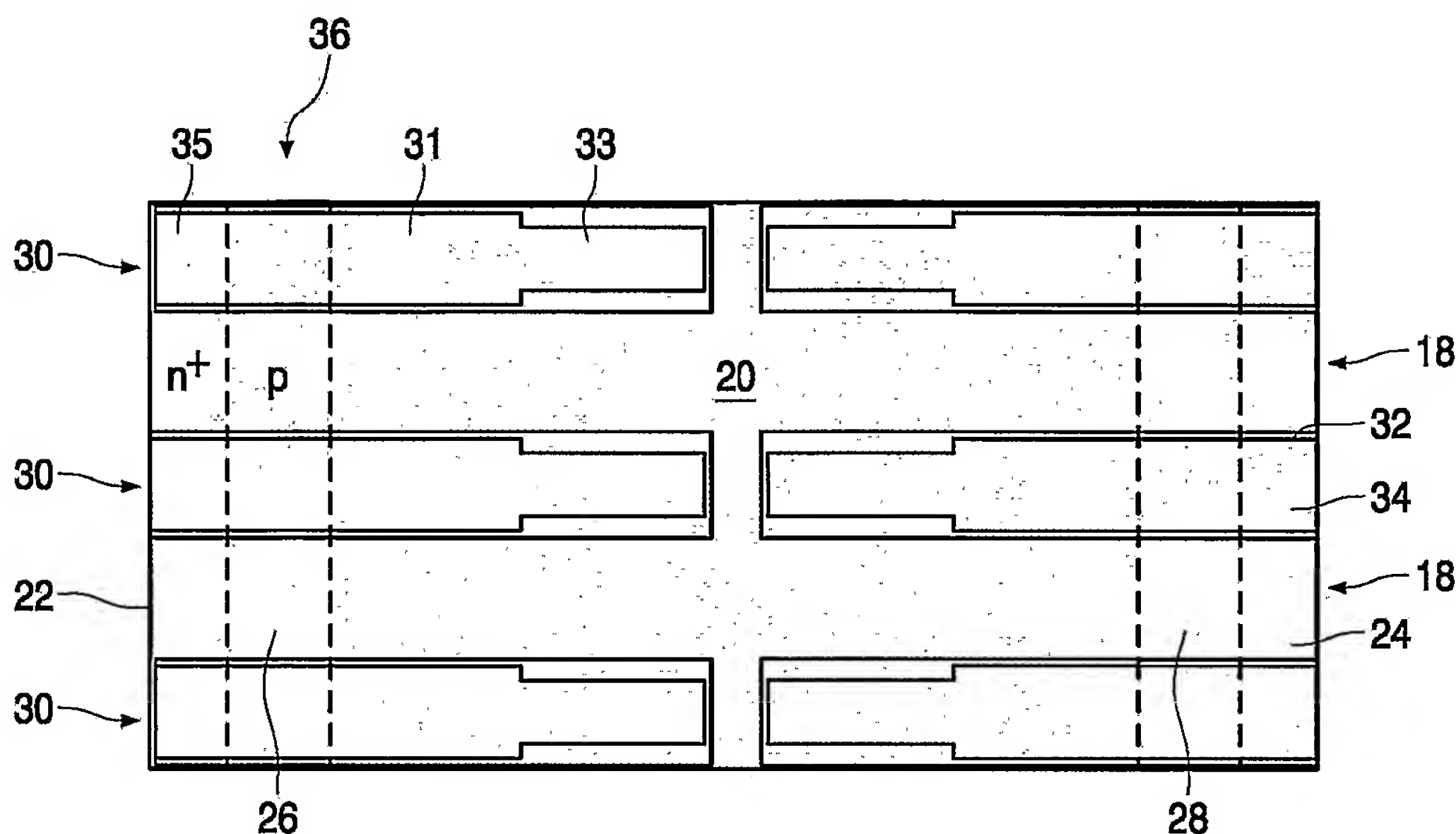




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(54) Title: LATERAL FIELD-EFFECT TRANSISTOR HAVING AN INSULATED TRENCH GATE ELECTRODE



(57) Abstract: A field-effect transistor having cells (18) each having a source region (22), source body region (26), drift region (20), drain body region (28) and drain region (24) arranged longitudinally, laterally alternating with structures to achieve a reduced surface field. In embodiments, the structures can include longitudinally spaced insulated gate trenches (35) defining a gate region (31) adjacent the source or drain region (22, 24) and a longitudinally extending potential plate region (33) adjacent the drift region (20). Alternatively, a separate potential plate region (33) or a longitudinally extending semi-insulating field plate (50) may be provided adjacent the drift region (20). The transistor is suitable for bi-directional switching.

**Declaration under Rule 4.17:**

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ,*

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